A Review on Two Stage Amplifier Using CMOS Technology

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Abstract: Operational amplifiers are an integral part of many analog and mixed signal systems. As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. This paper presents a review on two stage CMOS operational amplifier, which operates using 70nm CMOS technology. Voltage gain, phase gain and slew rate will be simulated for two stage amplifier model using 70nm technology. This study is carried out in P Spice tool.

Key words: CMOS Operational Amplifier, Voltage gain, Phase gain, Slew Rate, P Spice tool.

I. INTRODUCTION

CMOS stands for Complementary Metal Oxide Semiconductor is a technology for constructing integrated circuits and sometimes it is also referred as ComplementarySymmetry Metal Oxide Semiconductor (or COS-MOS). The words “complementary Symmetry” refers to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors for logic functions. High noise immunity and low static power consumption are the important characteristics of CMOS devices. Significant power in the CMOS can be drawn when the transistors device are switching between on and off states.

The rapid increasing complexity in chip structure has led to implementation of certain analog functions in Metal Oxide Semiconductor (“MOS”) technology. Existing CMOS technologies provide sufficient opportunity to integrate entire system into a single electronic circuit. As integrated circuit become more complex, it is essential to know the working of the circuit. Simulating a circuit without the knowledge of its working can lead to unproductive results. A schematic circuit; DC currents and W/L ratios are the three main outputs responsible for the electric design of CMOS analog circuits [1].

For the past half century, development of microelectronic has been really spectacular and the success results mainly because of a fundamental element “Silicon”. The MOS transistor is the principle element of this technological development and proves to be the support for the large scale integrated circuit design. But simultaneously, for improving the performance of MOS transistors in new generations, the complexity of integrated circuits has been increasing.

The application of CMOS technology can be found in microprocessors, microcontrollers, static RAM and other analog and digital circuits. CMOS circuits uses a combination of p-type and n-type metal-oxide-semiconductor field-effect transistor, logic gates and other circuits which can also be found in computers, telecommunications and other signal processing equipment. Now a day’s, CMOS technology has become dominant over bipolar technology for analog circuit design in a mixed signal system. This is due to the fact that industries are applying standard process technologies for implementing both analog and digital circuits on the same chip. [1]

The present packing densities for CMOS technologies allows the complete system to be integrated on a single chip. A wide range of applications requires the integration of analog and digital subsystems, which possess several significant challenges for the design of analog circuits in a typical digital environment. Currently, there has been growing demand of low power mixed signal integrated circuits for the mobile or wired communications and other applications. In these applications, supply voltage has to be scaled down for reducing overall power consumption.

The word ‘metal’ in the MOSFET is often called as misconer because the previously metal gate material consists a layer of poly silicon. Aluminum had been the gate material until the mid1970s, when poly silicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity as it is difficult to increase the speed of operation of transistors without metal gates. IGFET is another related term called as insulated-gate field-effect transistor, which is used synonymously with MOSFET, being more accurate since many "MOSFETs" use a gate that is not metal and a gate insulator that is not oxide [2].

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM and Intel, recently started using a chemical compound of silicon and germanium in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs. Research continues on creating insulators with acceptable electrical characteristics on other semiconductor material.

When a voltage is applied between the gate and body terminals, the generated electric field penetrates through the oxide and creates an “inversion layer” or "channel" at the semiconductor-insulator interface. The inversion channel is of the same type, P-type or N-type, as the source and drain, thus it provides a channel through which current can pass. Varying the voltage between the gate and body modulates the conductivity of this layer and thereby controls the current flow between drain and source. A variety of symbols are used for the MOSFET. The basic design is generally a line for the channel with
the source and drain leaving it at right angles and then bending back at right angles into the same direction as the channel. Sometimes three line segments are used for enhancement mode and a solid line for depletion mode. Another line is drawn parallel to the channel for the gate[2]

![Figure 1: Comparison of Enhancement-mode and Depletion-mode MOSFET and JFET Symbols](image)

The bulk connection as shown connected to the back of the channel with an arrow indicating PMOS or NMOS. Arrows always point from P to N, so an NMOS (N-channel in P-well or P-substrate) has the arrow pointing in (from the bulk to the channel). If the bulk is connected to the source (as is generally the case with discrete devices) it is sometimes angled to meet up with the source leaving the transistor. If the bulk is not shown (as is often the case in IC design as they are generally common bulk) an inversion symbol is sometimes used to indicate PMOS, alternatively an arrow on the source may be used in the same way as for bipolar transistors (out for n-MOS, in for p-MOS). [2]

CMOS CIRCUITS

The MOSFET is used in digital CMOS logic which uses p- and n-channel MOSFETs as building blocks. Overheating is a major concern in integrated circuits since ever more transistors are packed into ever smaller chips. CMOS logic reduces power consumption because no current flows (ideally), and thus no power is consumed, except when the inputs to logic gates are being switched. CMOS accomplishes this current reduction by complementing every n-MOSFET with a p-MOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the n-MOSFET to conduct and the p-MOSFET not to conduct and a low voltage on the gates causes the reverse. During the switching time as the voltage goes from one state to another, both MOSFETs will conduct briefly. This arrangement greatly reduces power consumption and heat generation.

II. LITERATURE REVIEW

Chien-Chih Ho et al (2003) presented a fully integrated two-stage 1.9 GHz class-E amplifier, implemented by 0.18 μm CMOS technologies. By using the switching operation mode of a class-E amplifier, the dc power dissipation can be reduced, and this amplifier delivers a 16.3 dBm output power at 1.9 GHz, with a maximum power-added efficiency (PAE) of 70% from a 2V dc supply voltage. This monolithic amplifier includes the matching and biasing circuit, where no external components are required.

Christian Falconi (2003) summarized the results of dynamic op amp matching which is a very attractive technique for the implementation of accurate analog circuits in low voltage low power CMOS systems. He concluded that when comparing the chopper and with traditional dynamic element matching, it allows the compensation of the finite op amp gain and, in comparison with auto zero, it gives better noise performance.

S.S Jamuar and Tang Kia Kit (2004) described the design of a CMOS based low voltage op-amp. The low voltage op-amp can be operated with supply voltage of ±1V. It has unity-gain bandwidth of 18 MHz without compensation and slew rate of 25 V/μs with 10 pF capacitive load. A compensation network has been implemented, which enables the op-amp’s unity-gain bandwidth to increase till 24 MHz. Under no load condition, it gives a bandwidth of 576 MHz. All of the simulations in this project are using 0.8 μm CMOS technology.

Shem-Tov, et al (2004) presented a method for the design of high speed CMOS operational amplifiers. The op-amp consists of an operational trans-conductance amplifier followed by an output buffer. The OTA is compensated with a capacitor connected between the input and output of the buffer. An op-amp is designed in a 0.18 μm standard digital CMOS technology and exhibits 86 dB DC gains. The unity gain frequency and phase margin are 392 MHz and 73˚, respectively, for a parallel combination of 2 pF and 1 kΩ load. As compared to the conventional approach, the proposed compensation method results in a 1.5 times increase in unity gain frequency and a 35˚ improvement in the phase margin under the same load condition.

Jirayuth Mahattanakul and Jamorn Chutichatuporn (2005) presented basic two-stage CMOS op-amp design procedure that provides the circuit designer with a means to strike a balance between two important characteristics in electronic circuit design, namely noise performance and power consumption. It is shown that, unlike the previously reported design procedures, the proposed design step allows op-amp designers to trade between noise performance and power consumption with greater flexibility. In order to verify the viability of the proposed design step, SPICE simulation results of the op-amp designed by the proposed procedure, under a variety of temperature and process conditions, are given.

Aimad El Mourabit et al (2005) proposed a novel configuration of linearized sub threshold operational trans-conductance amplifier for low-power, low-voltage, and low-frequency applications. By using multiple input floating-gate (MIFG) MOS devices and implementing acubic-distortion-term-canceling technique, the linear range of the OTA is up to 1.1Vpp under a 1.5 V supply for less than 1% of trans-
conductance variation, according to testing results from a circuit designed in a double-poly, 0.8 μm, CMOS process. The power consumption of the OTA remains below 1 μW for biasing currents in the range between 1 to 20 nA. The offset voltage due to secondary effects (contributed by parasitic capacitances, errors and mismatches of parameters, charge entrapment, etc.) is of the order of a few ten millivolts, and can be canceled by adjusting biasing voltages of input MIFG MOS transistors.

Madhu Bhaskaran et al (2006) discussed a CMOS operational amplifier at ±3 V supply, with rail-to-rail input and output performance. The trade-off between rail-to-rail performance and power consumption, in terms of bias current is observed. Simulation results with SPICELevel 3 models, using Cadence tools, are discussed and compared with other op-amps. The proposed circuit exhibits high speed with Slew Rate of 49.24 V/μs, better rejection ratios and offset performance, and consumes a power of 25.44 mW for rail-to-rail performance.

Vishal Saxena and R. Jacob Baker (2006) presented the design of CMOS op-amps using indirect feedback compensation technique. The indirect feedback compensation results in much faster and low power op-amps, significant reduction in the layout size and better power supply noise rejection. Conclusion of the paper is indirect feedback compensation is a practical and superior technique for compensation of op-amps and results in faster and low power op-amps with much smaller layout size. The indirect feedback compensation can also be extended to three (or more) stage op-amps.

Raj Kumar Tiwari et al (2009) reported a new model for high performance CMOS differential amplifier. The proper selection of device parameters has been playing an important role in the design of differential amplifier. This model is simulated in SPICE simulator and optimized device parameters. This circuit best suited for low voltage and high common mode rejection ratio (CMRR) applications. The input voltage can be applied between -3.14 volts to +3.14 volts and its performance is better up to 5MHz. The circuit can be used in design of low voltage and CMRR operational amplifiers, Operational trans-conductance amplifiers, Voltage controlled oscillators (VCO).

Vishal Saxena and Jacob Baker (2009) discussed new design techniques for the realization of three-stage op-amps. The proposed and experimentally verified op-amps, fabricated in 500 nm CMOS, typically exhibit 30 MHz unity-gain frequencies, near 100 ns transient settling and 72° phase-margin for 500 pF load. This results in significantly higher op-amp performance metrics over the traditional op-amp designs while at the same time having smaller layout area.

Nabhan and Moussa Abdallah Ismail (2010) designed a two-stage operational amplifier simulated and fabricated using a UMC 0.5 μm 2P2M CMOS technology. This chip includes a compensation technique to ensure stability and zero systematic input-offset-voltage. The fabricated chip achieves a 84 dB open loop gain, a 24 V μS slew rate, a 84 dB CMRR utilizing a capacitive load of 5 pF, a 30 MHz unity gain frequency and consumes 2.8 mW from a 2.5 V power supply. The proposed chip, which is the first available CMOS operational amplifier in Jordan as the authors are aware, is well-suited to low-voltage applications since it does not require cascade output stages.

Priyanka Kakoty (2011) presented a method for the design of a high frequency CMOS operational amplifier which operates at 3 V power supply using TSMC 0.18 micron CMOS technology. The op-amp designed is a two-stage CMOS op-amp followed by an output buffer. This operational trans-conductance amplifier employs a Miller capacitor and is compensated with a current buffer compensation technique. The unique behavior of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The op-amp is designed to exhibit a unity gain frequency of 2.02 GHz and exhibits a gain of 49.02 dB with a 60.5° phase margin. As compared to the conventional approach, the proposed compensation method results in a higher unity gain frequency under the same load condition. Design has been carried out in Tanner tools.

Bakkem Sateesh (2012) design a Low-Voltage, Low-Power and High-Gain Operational Amplifier used for Data Conversion process. These Data Converters are used in Biomedical and Telecommunication applications. This work presents the optimized architecture of an operational amplifier. The characteristics are verified by using 0.18μm CMOS technology and also outlines the performance of an op-amp at supply voltage 1.2V.

The simulation results show that the Open Loop Gain≥79dB, Unity Gain Frequency≥110MHz, Slew Rate=175v/μs, CMRR≥89dB, PSRR≥75dB, ICMR=0 to 1.2v(Rail to Rail), Settling Time≤10ns, Output Swing= close to rail and Input Offset Voltage=0.001μv.

Shahid Khan (2014) designed a two stage CMOS operational amplifier, which operates at ±1.8V power supply using TSMC 0.18um CMOS technology. The OP-AMP designed exhibit unity gain frequency of 12.6 MHz, and gain of 55.5dB with 300uw power dissipation. The gain margin and phase margin of OP-AMP was 45° and 60° respectively. Design and simulation was carried out in P Spice tool.

III. RESEARCH METHODOLOGY

The methodology which is adopted for carrying out research work is as follows:

- Literature review
- Identification of special issues related to topic.
- Carry out study and analysis of operational amplifier using NMOS, PMOS & CMOS.
- Analyzing the circuits in 180nm,100nm and 70 nm technology and obtain a conclusion for high gain Operational amplifier.
- Comparative analysis among present study and previously reported is done
- Tanner EDA simulation will be used for implementation in 180nm,100nm and 70 nm technology.

IV. CONCLUSIONS
This work presents a comparative study and analysis of the CMOS operational amplifier using 180nm, 100nm, and 70nm CMOS technologies. The circuits named two-stage single ended op-amp have been simulated in Tanner EDA. The variation of parameters like gain, phase margin, and slew rate with respect to input voltage and VDD has been simulated using the tool. For the two-stage op-amp in 180nm technologies with Vdd=5V and Vss=-1V, gain is 43.5 dB, phase margin is 82 degrees and slew rate 15V/us for rising edge has been observed. For the two-stage op-amp in 100nm technologies with Vdd=5V and Vss=-1V, gain is 34 dB, phase margin is 102 degrees and slew rate 25V/us for rising edge has been observed. I will derive same parameter in my dissertation using 70nm technology.

REFERENCES